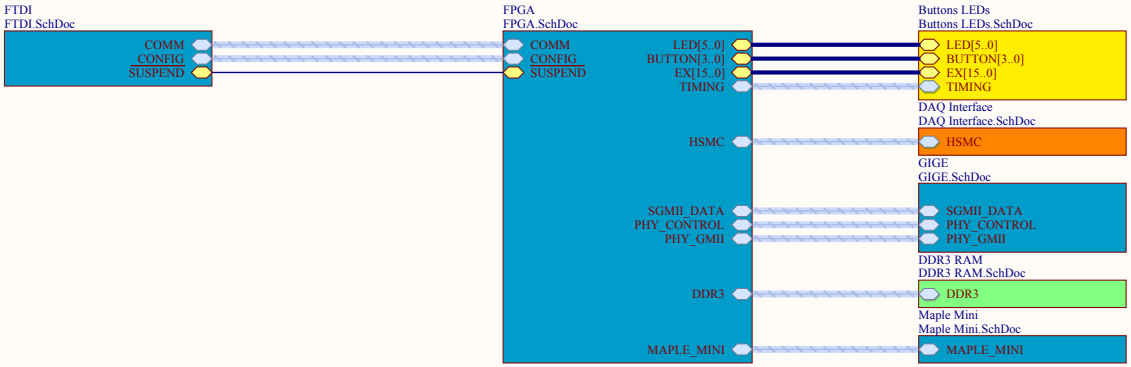
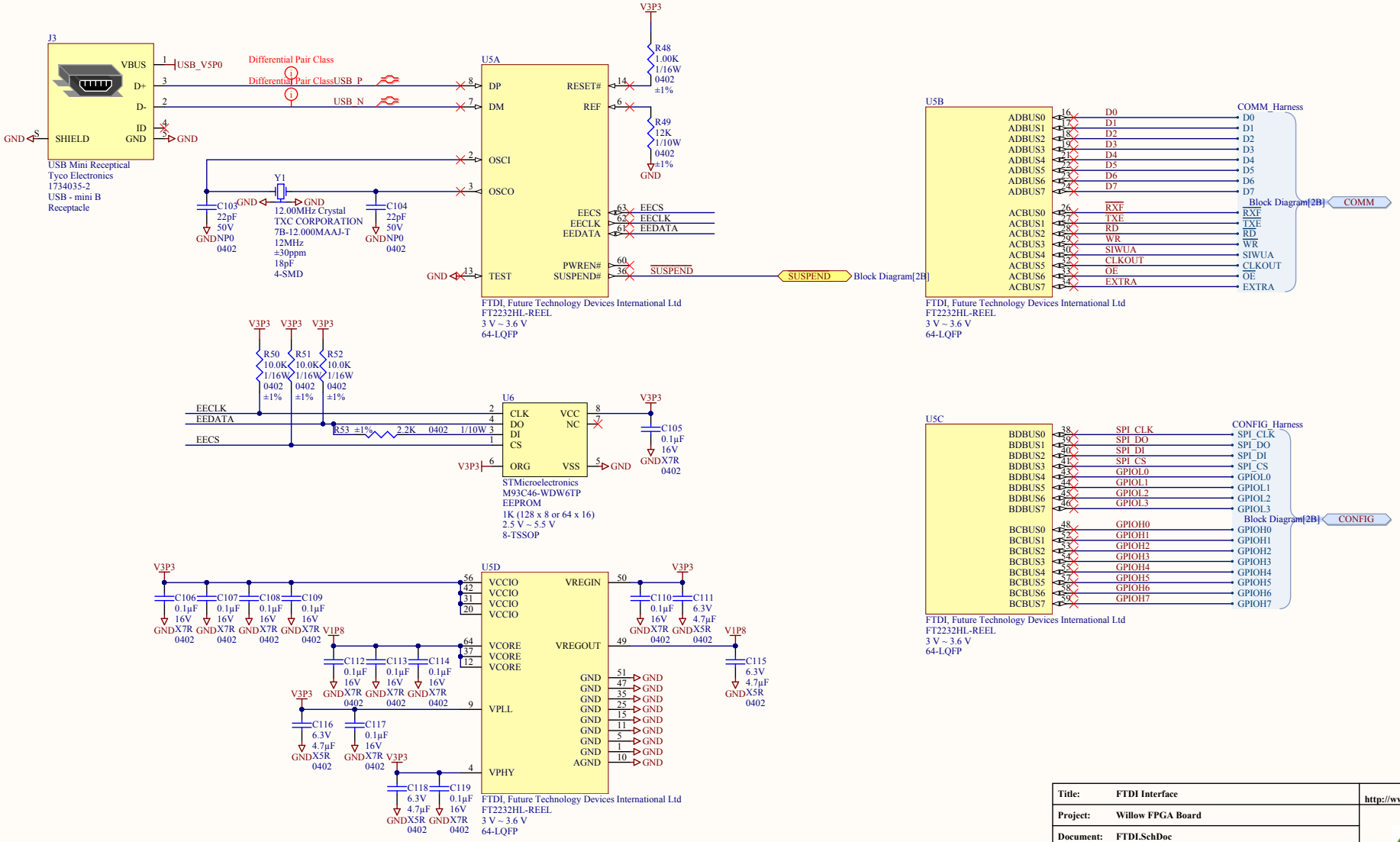
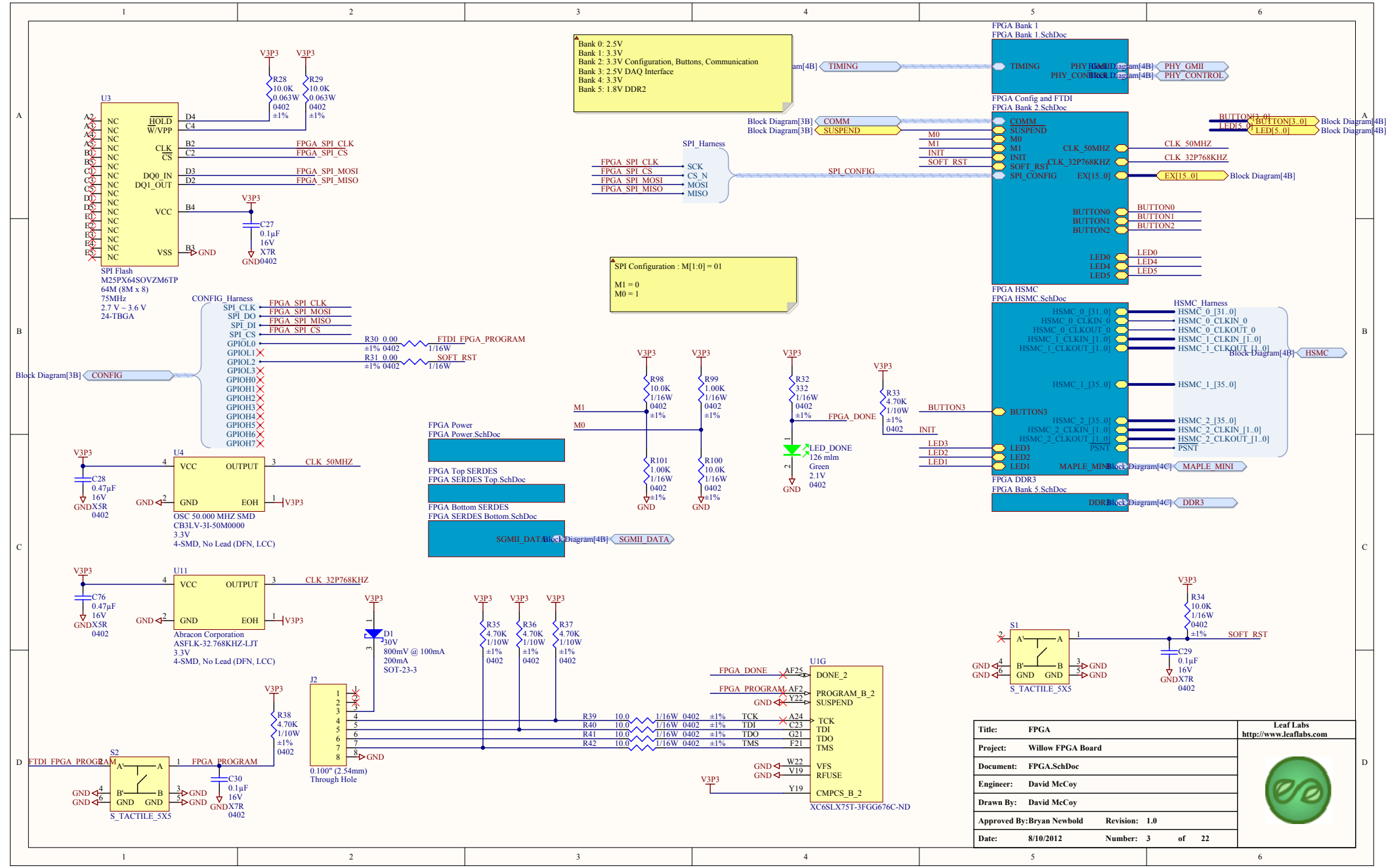
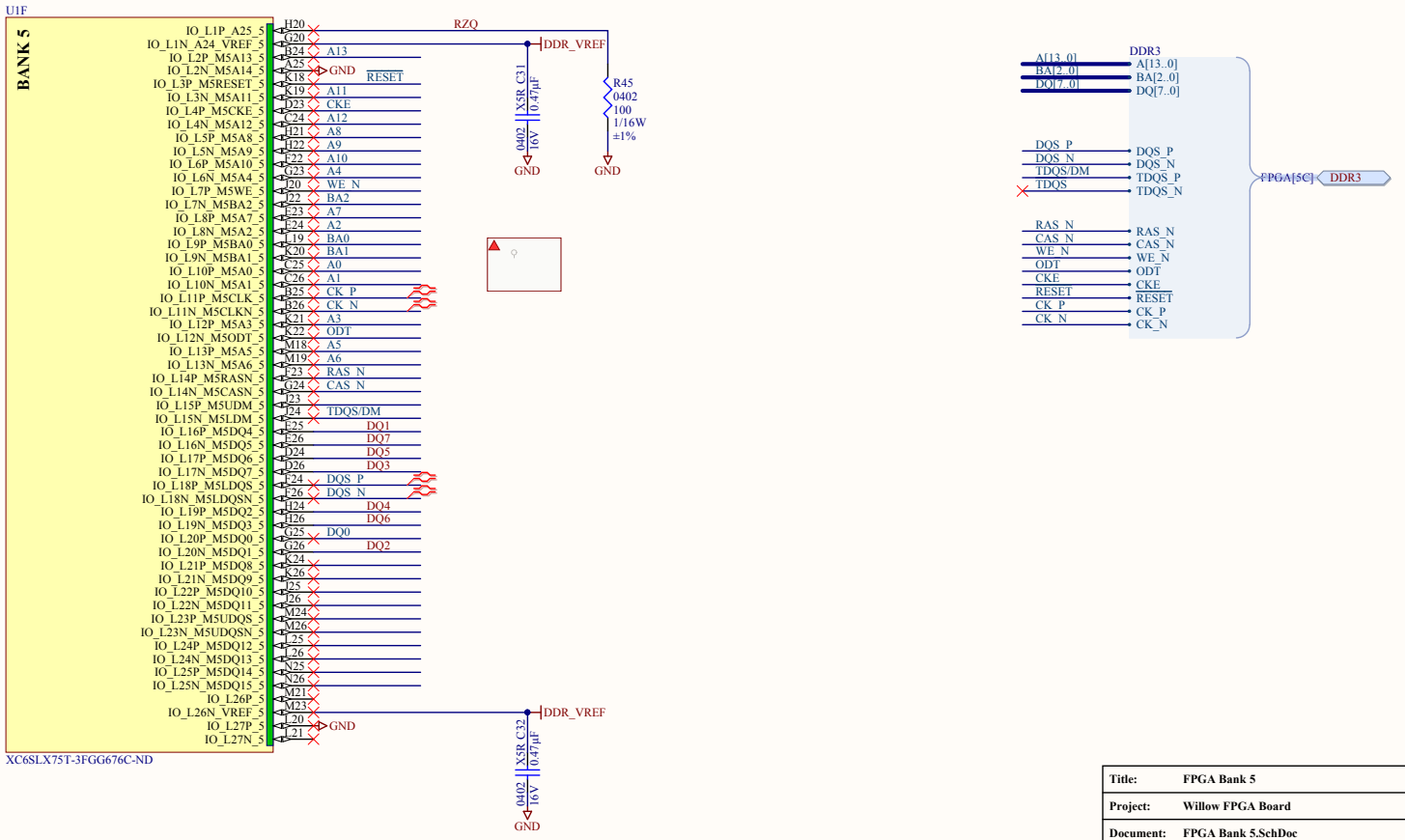


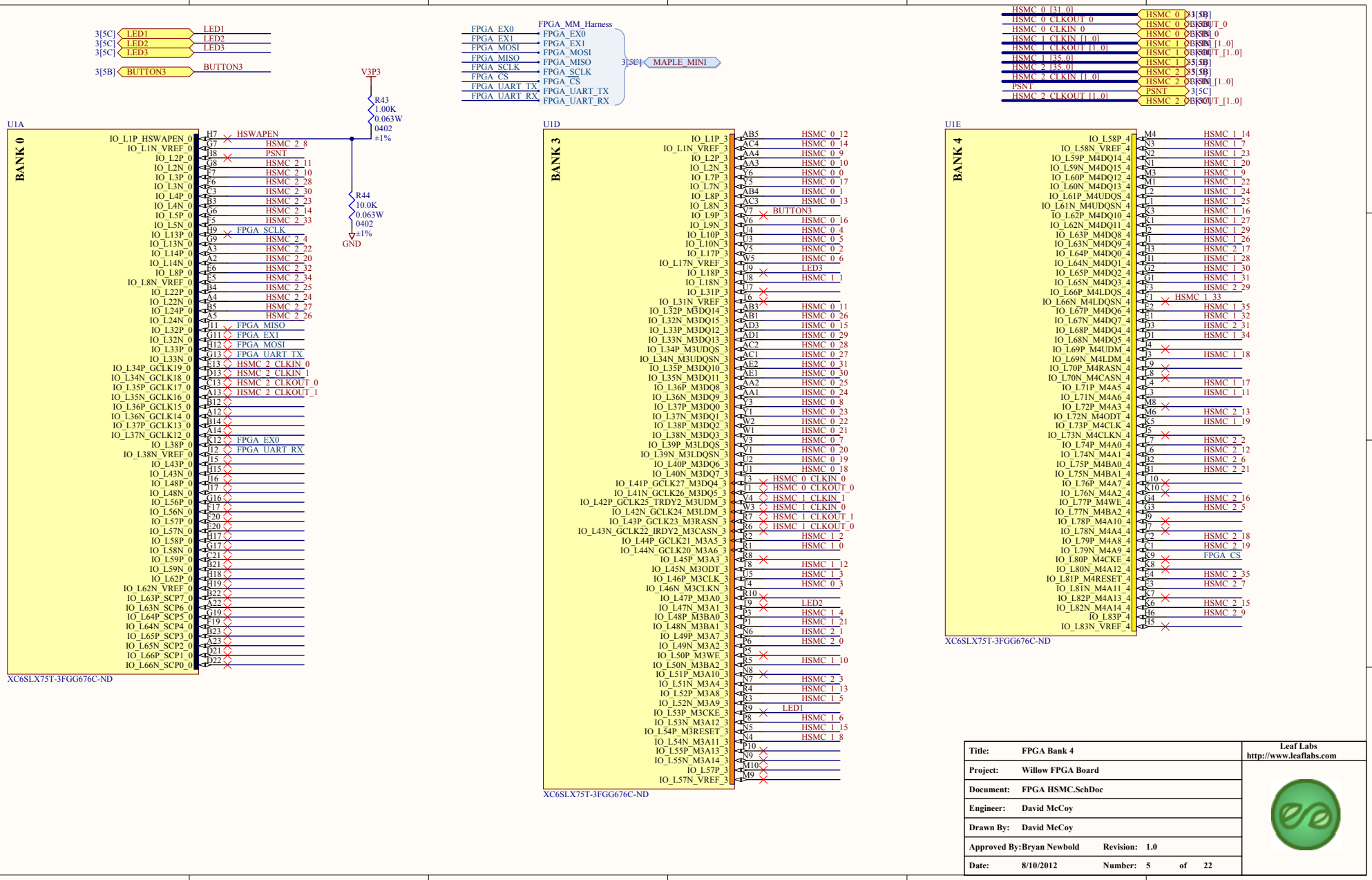
Title:	**Block Diagram**			**Leaf Labs** **http://www.leaflabs.com**
Project:	**Willow FPGA Board**			
Document:	**Block Diagram.SchDoc**			
Engineer:	**David McCoy**			
Drawn By:	**David McCoy**			
Approved By:	**Bryan Newbold**	**Revision:**	**1.0**	
Date:	**8/10/2012**	**Number:**	**1 of 22**	


J3
VBUS
D+
D-
ID
SHIELD
GND
USB_V5P0
USB_P
USB_N
Differential Pair Class
USB Mini Receptical
Tyco Electronics
1734035-2
USB - mini B
Receptacle
U5A
DP
DM
OSCI
OSCO
TEST
RESET#
REF
EECS
EECLK
EEDATA
PWREN#
SUSPEND#
V3P3
R48
1.00K
1/16W
0402
±1%
R49
12K
1/10W
Y1
12.00MHz Crystal
TXC CORPORATION
7B-12.000MAAJ-T
12MHz
±30ppm
18pF
4-SMD
C103
C104
22pF
50V
NP0
FTDI, Future Technology Devices International Ltd
FT2232HL-REEL
3 V ~ 3.6 V
64-LQFP
SUSPEND
Block Diagram[2B]
U5B
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
ACBUS0
ACBUS1
ACBUS2
ACBUS3
ACBUS4
ACBUS5
ACBUS6
ACBUS7
D0
D1
D2
D3
D4
D5
D6
D7
RXF
TXE
RD
WR
SIWUA
CLKOUT
OE
EXTRA
COMM_Harness
COMM
R50
R51
R52
10.0K
1/16W
0402
±1%
U6
CLK
DO
DI
CS
ORG
VCC
NC
VSS
R53 ±1% 2.2K 0402 1/10W
C105
0.1µF
16V
X7R
STMicroelectronics
M93C46-WDW6TP
EEPROM
1K (128 x 8 or 64 x 16)
2.5 V ~ 5.5 V
8-TSSOP
U5C
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
BCBUS0
BCBUS1
BCBUS2
BCBUS3
BCBUS4
BCBUS5
BCBUS6
BCBUS7
SPI_CLK
SPI_DO
SPI_DI
SPI_CS
GPIOL0
GPIOL1
GPIOL2
GPIOL3
GPIOH0
GPIOH1
GPIOH2
GPIOH3
GPIOH4
GPIOH5
GPIOH6
GPIOH7
CONFIG_Harness
CONFIG
U5D
VCCIO
VREGIN
VCORE
VREGOUT
VPLL
VPHY
AGND
C106
C107
C108
C109
C110
C111
C112
C113
C114
C115
C116
C117
C118
C119
0.1µF
4.7µF
6.3V
V1P8
Title: FTDI Interface
Project: Willow FPGA Board
Document: FTDI.SchDoc
Engineer: David McCoy
Drawn By: David McCoy
Approved By: Bryan Newbold
Revision: 1.0
Date: 8/10/2012
Number: 2 of 22
Leaf Labs
http://www.leaflabs.com


Bank 0: 2.5V
Bank 1: 3.3V
Bank 2: 3.3V Configuration, Buttons, Communication
Bank 3: 2.5V DAQ Interface
Bank 4: 3.3V
Bank 5: 1.8V DDR2
SPI Configuration : M[1:0] = 01
M1 = 0
M0 = 1
FPGA Bank 1
FPGA Bank 1.SchDoc
FPGA Config and FTDI
FPGA Bank 2.SchDoc
FPGA HSMC
FPGA HSMC.SchDoc
FPGA DDR3
FPGA Bank 5.SchDoc
FPGA Power
FPGA Power.SchDoc
FPGA Top SERDES
FPGA SERDES Top.SchDoc
FPGA Bottom SERDES
FPGA SERDES Bottom.SchDoc
SPI_Harness
CONFIG_Harness
HSMC_Harness
SPI Flash
M25PX64SOVZM6TP
64M (8M x 8)
75MHz
2.7 V ~ 3.6 V
24-TBGA
OSC 50.000 MHZ SMD
CB3LV-3I-50M0000
3.3V
4-SMD, No Lead (DFN, LCC)
Abracon Corporation
ASFLK-32.768KHZ-LJT
3.3V
4-SMD, No Lead (DFN, LCC)
D1
30V
800mV @ 100mA
200mA
SOT-23-3
0.100" (2.54mm)
Through Hole
S_TACTILE_5X5
XC6SLX75T-3FGG676C-ND
Title: FPGA
Project: Willow FPGA Board
Document: FPGA.SchDoc
Engineer: David McCoy
Drawn By: David McCoy
Approved By: Bryan Newbold
Revision: 1.0
Date: 8/10/2012
Number: 3 of 22
Leaf Labs
http://www.leaflabs.com



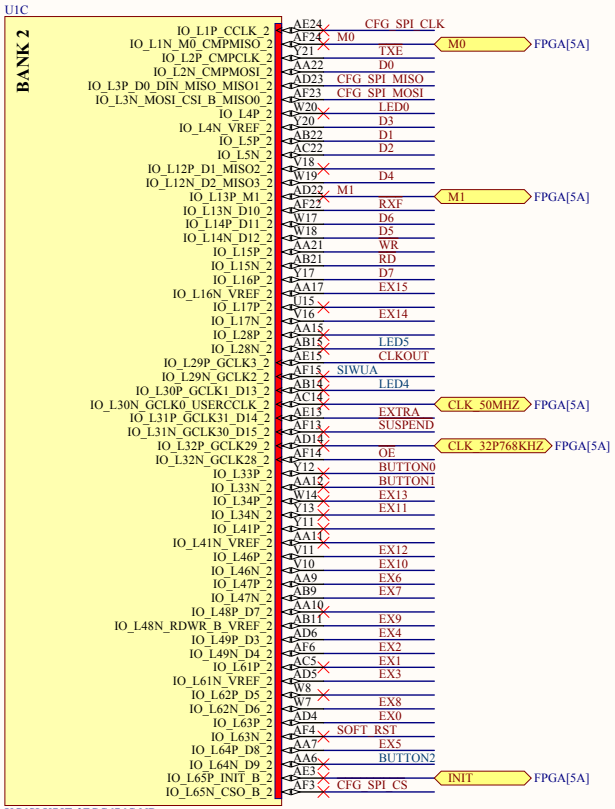
Title:	**FPGA Bank 5**		**Leaf Labs** http://www.leaflabs.com
Project:	**Willow FPGA Board**		
Document:	**FPGA Bank 5.SchDoc**		
Engineer:	**David McCoy**		
Drawn By:	**David McCoy**		
Approved By:	**Bryan Newbold**	**Revision:** **1.0**	
Date:	**8/10/2012**	**Number:** **4** **of** **22**	

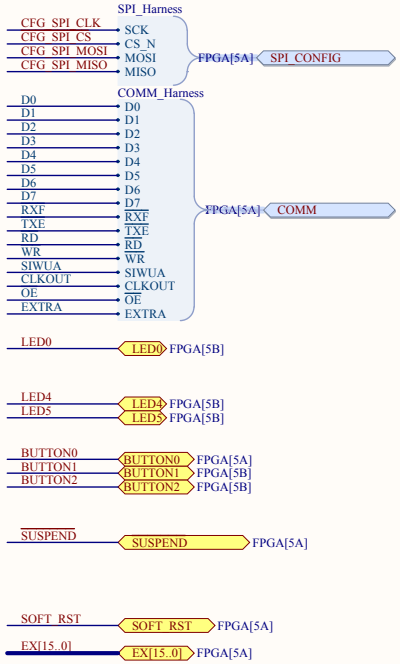

3[5C] LED1
3[5C] LED2
3[5C] LED3
3[5B] BUTTON3
V3P3
R43
1.00K
0.063W
0402
±1%
R44
10.0K
0.063W
0402
±1%
GND
U1A
BANK 0
XC6SLX75T-3FGG676C-ND
FPGA_EX0
FPGA_EX1
FPGA_MOSI
FPGA_MISO
FPGA_SCLK
FPGA_CS
FPGA_UART_TX
FPGA_UART_RX
FPGA_MM_Harness
3[5C]
MAPLE_MINI
U1D
BANK 3
XC6SLX75T-3FGG676C-ND
HSMC_0_[31..0]
HSMC_0_CLKOUT_0
HSMC_0_CLKIN_0
HSMC_1_CLKIN_[1..0]
HSMC_1_CLKOUT_[1..0]
HSMC_1_35_0
HSMC_2_35_0
HSMC_2_CLKIN_[1..0]
PSNT
HSMC_2_CLKOUT_[1..0]
U1E
BANK 4
XC6SLX75T-3FGG676C-ND
Title: FPGA Bank 4
Project: Willow FPGA Board
Document: FPGA HSMC.SchDoc
Engineer: David McCoy
Drawn By: David McCoy
Approved By: Bryan Newbold
Revision: 1.0
Date: 8/10/2012
Number: 5 of 22
Leaf Labs
http://www.leaflabs.com

Pay attention to the configuration pins

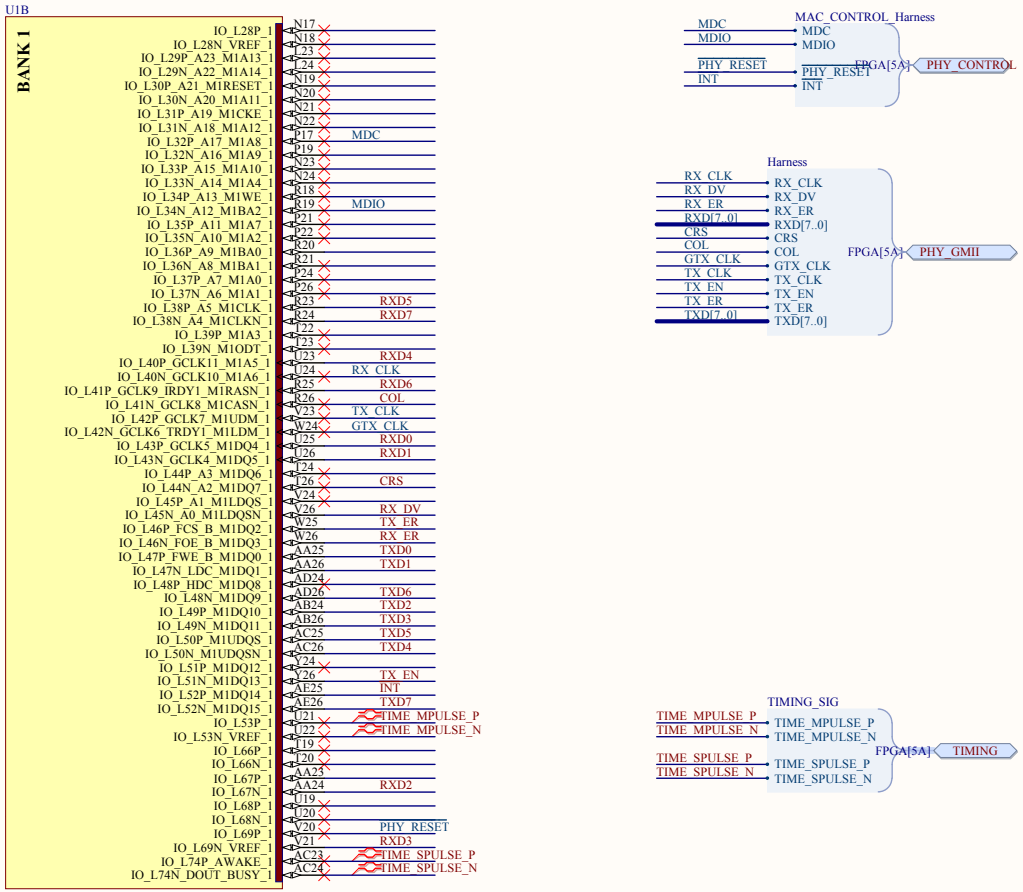
Connct 50MHz Clock to a GCLK pin!

Connct CLKOUT to a GCLK pin!

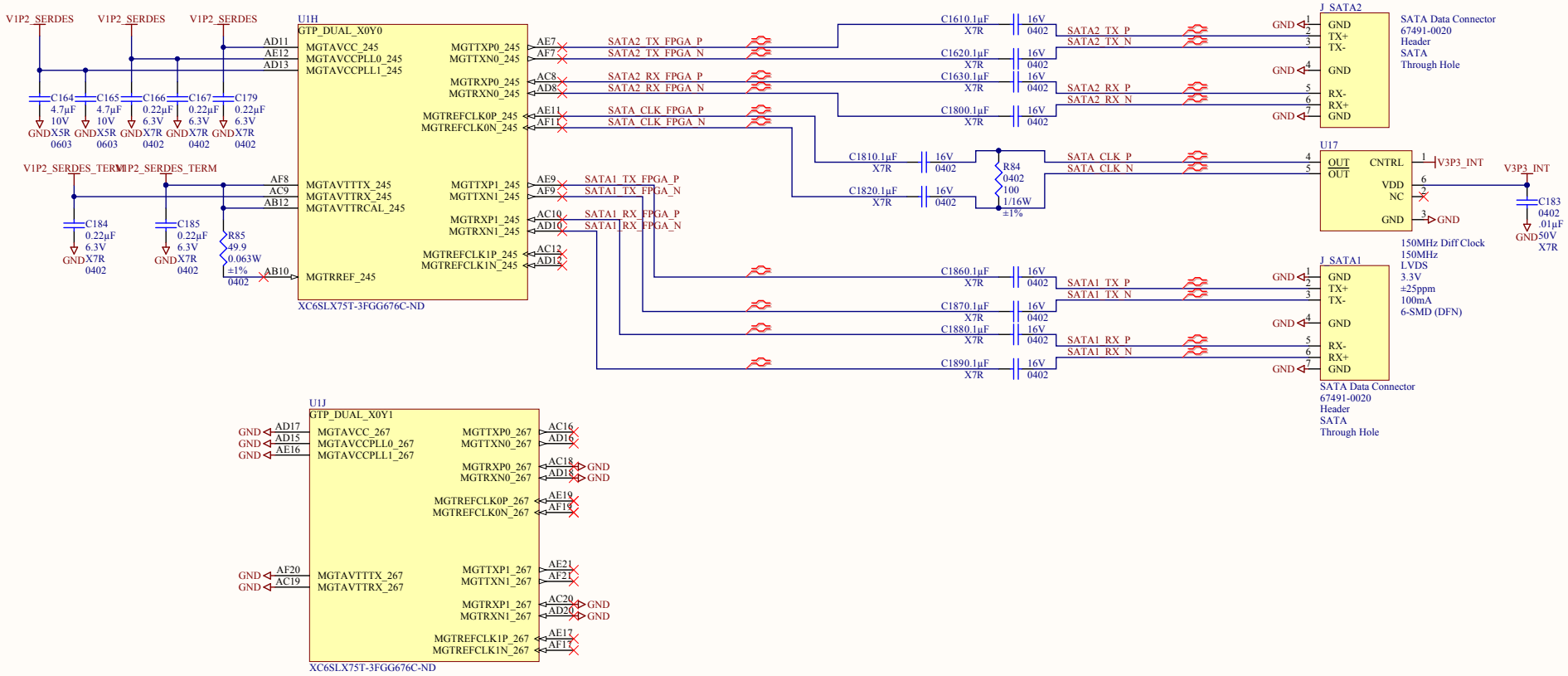




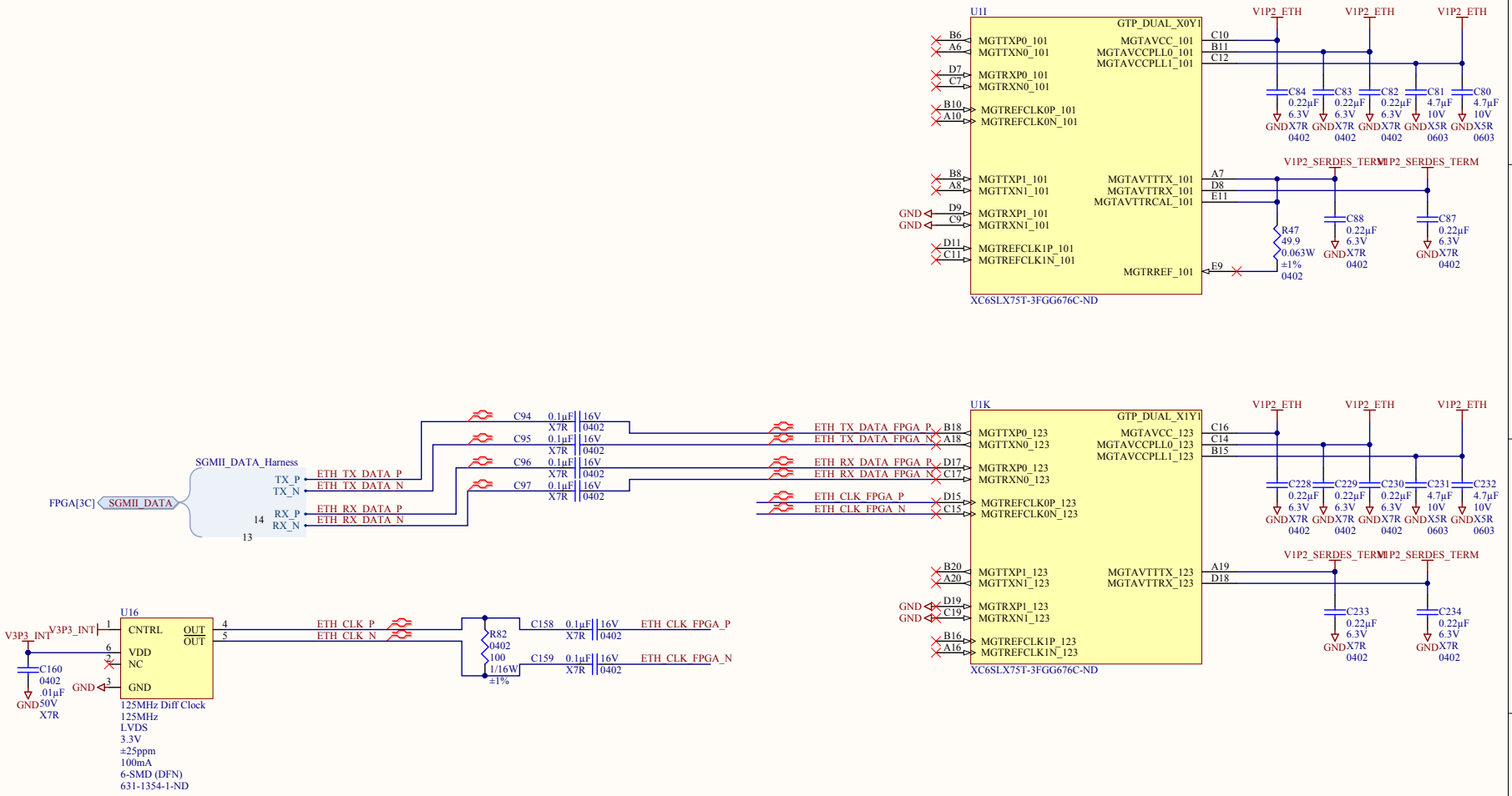
Title:	**FPGA Bank 2**		**Leaf Labs http://www.leaflabs.com**
Project:	**Willow FPGA Board**		
Document:	**FPGA Bank 2.SchDoc**		
Engineer:	**David McCoy**		
Drawn By:	**David McCoy**		
Approved By:	**Bryan Newbold**	**Revision:** **1.0**	
Date:	**8/10/2012**	**Number:** **6** **of** **22**	



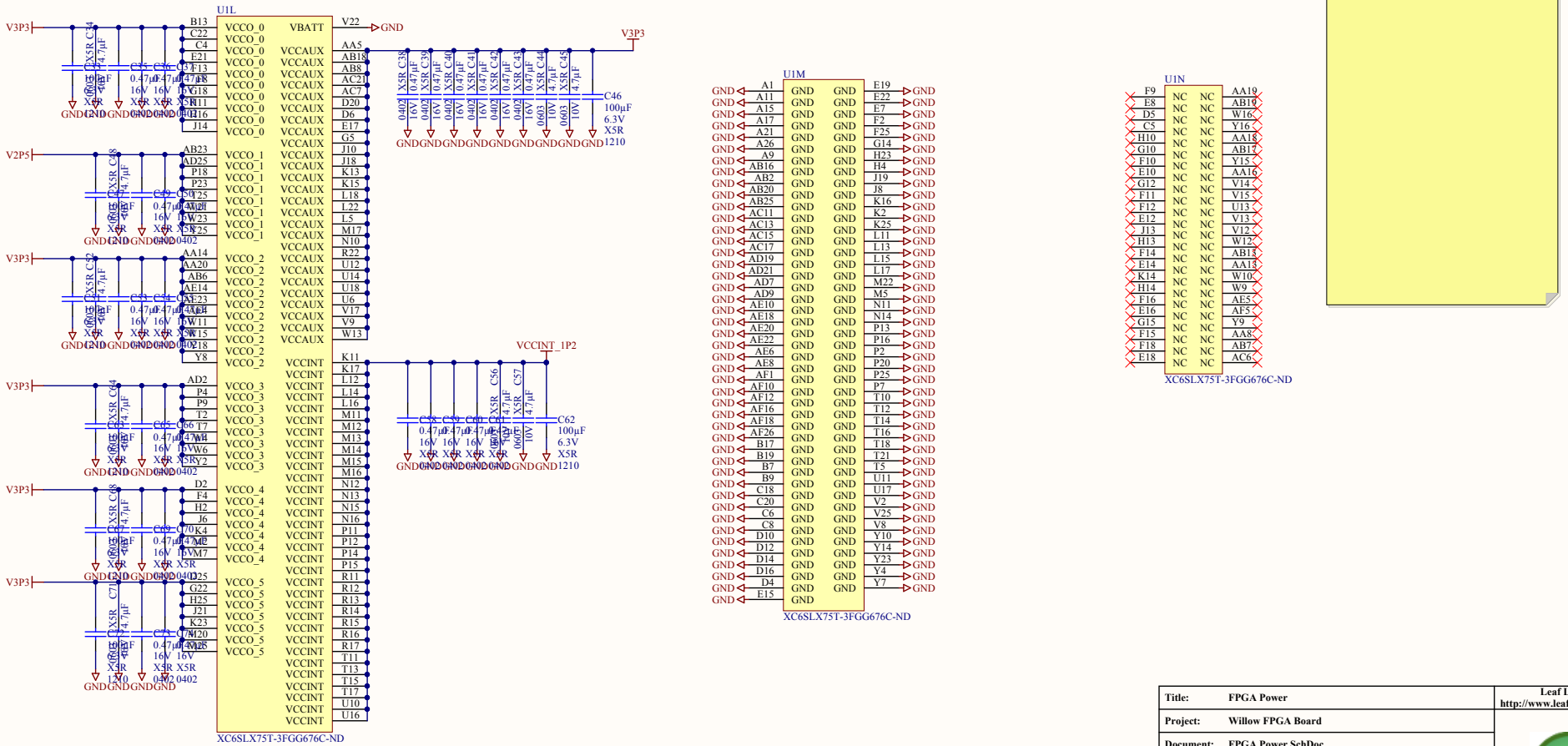
Title:	**FPGA Bank 1**		**Leaf Labs** http://www.leaflabs.com
Project:	**Willow FPGA Board**		
Document:	**FPGA Bank 1.SchDoc**		
Engineer:	**David McCoy**		
Drawn By:	**David McCoy**		
Approved By:	**Bryan Newbold**	**Revision:** **1.0**	
Date:	**8/10/2012**	**Number:** **7** **of** **22**	



Title:	FPGA GTP Top		Leaf Labs http://www.leaflabs.com
Project:	Willow FPGA Board		
Document:	FPGA SERDES Top.SchDoc		
Engineer:	David McCoy		
Drawn By:	David McCoy		
Approved By:	Bryan Newbold	Revision: 1.0	
Date:	8/10/2012	Number: 8 of 22	

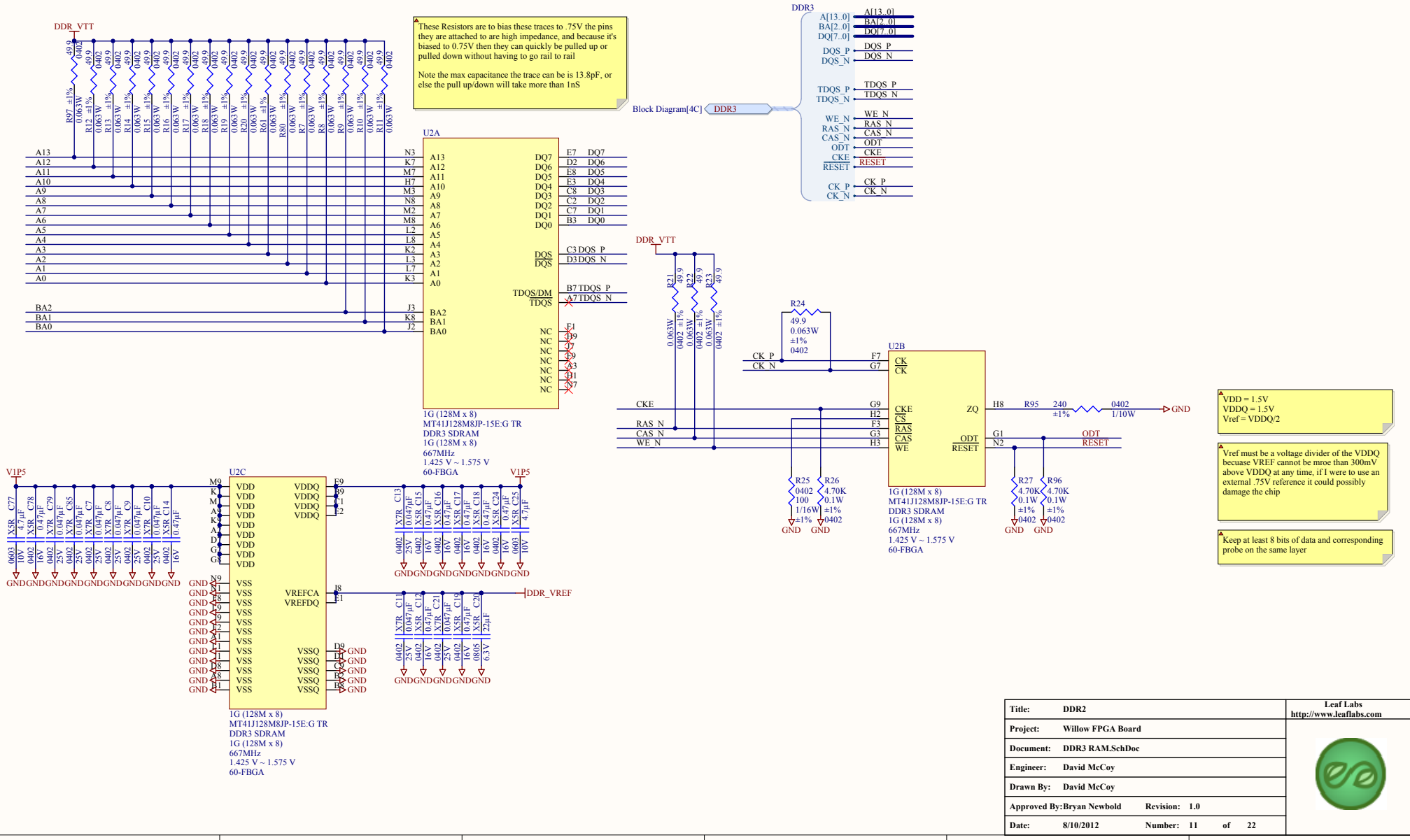


Title:	**FPGA GTP Bottom**		**Leaf Labs** http://www.leaflabs.com
Project:	**Willow FPGA Board**		
Document:	**FPGA SERDES Bottom.SchDoc**		
Engineer:	**David McCoy**		
Drawn By:	**David McCoy**		
Approved By:	**Bryan Newbold**	**Revision:** **1.0**	
Date:	**8/10/2012**	**Number:** **9** **of** **22**	

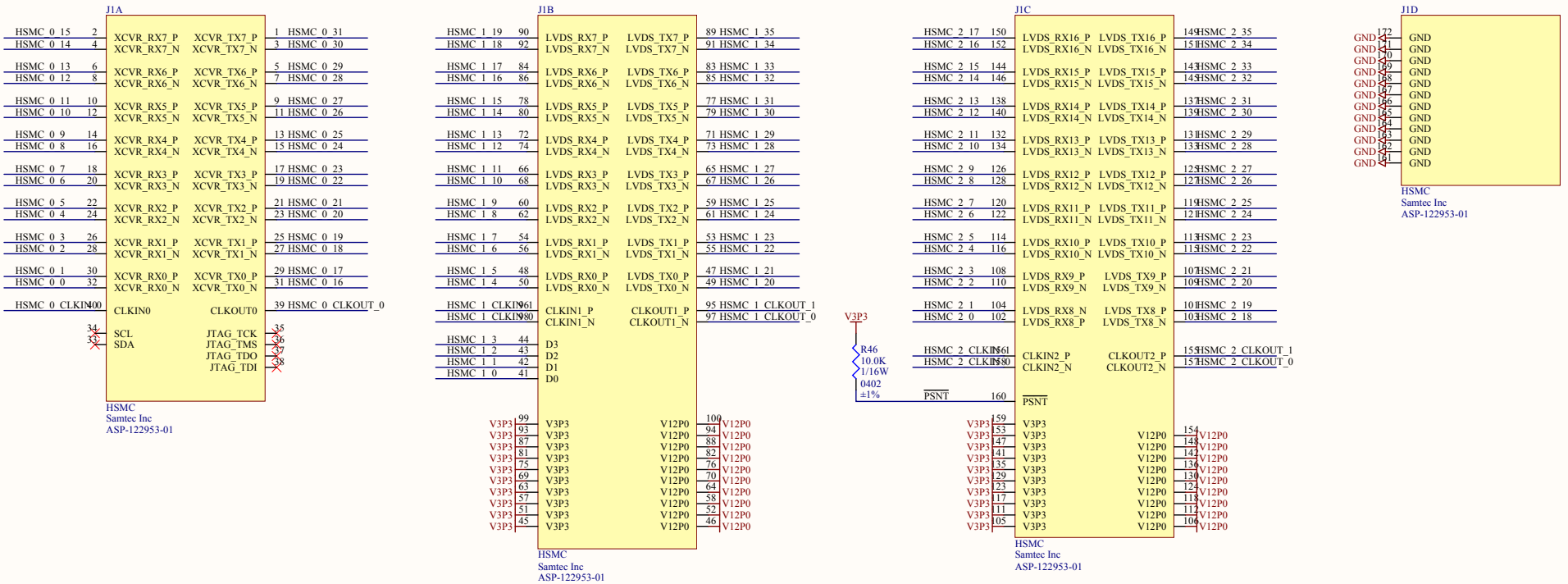


Title:	FPGA Power		Leaf Labs http://www.leaflabs.com
Project:	Willow FPGA Board		
Document:	FPGA Power.SchDoc		
Engineer:	David McCoy		
Drawn By:	David McCoy		
Approved By:	Bryan Newbold	Revision: 1.0	
Date:	8/10/2012	Number: 10 of 22	

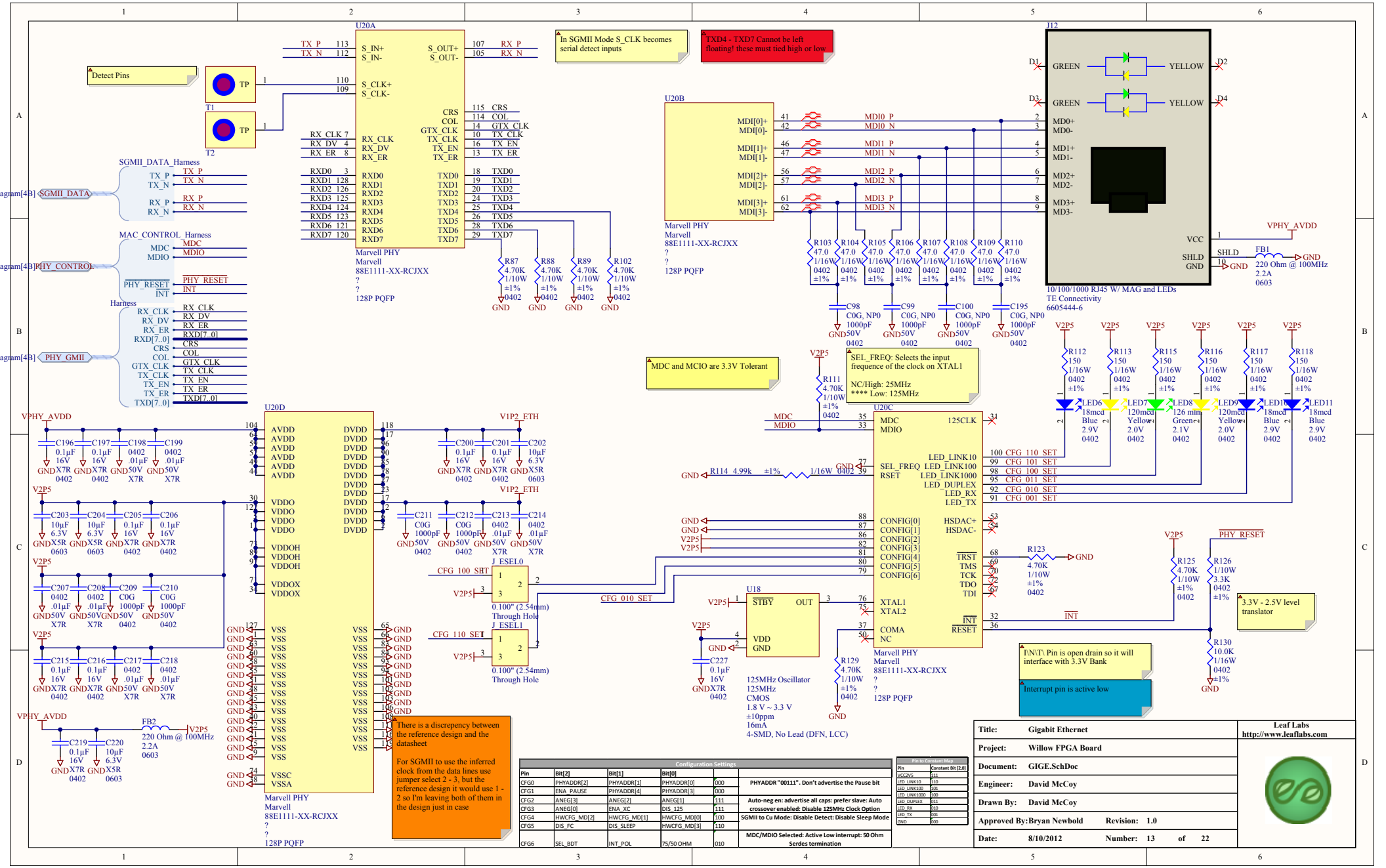
Power = 840mW Per DDR2

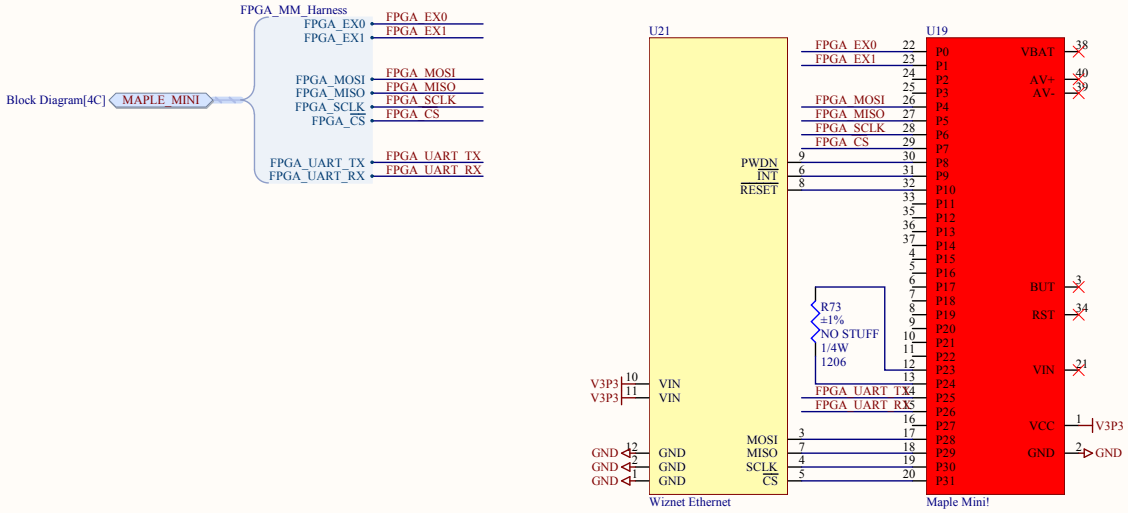


Title:	**DDR2**		**Leaf Labs** http://www.leaflabs.com
Project:	**Willow FPGA Board**		
Document:	**DDR3 RAM.SchDoc**		
Engineer:	**David McCoy**		
Drawn By:	**David McCoy**		
Approved By:	**Bryan Newbold**	**Revision:** **1.0**	
Date:	**8/10/2012**	**Number:** **11** **of** **22**	

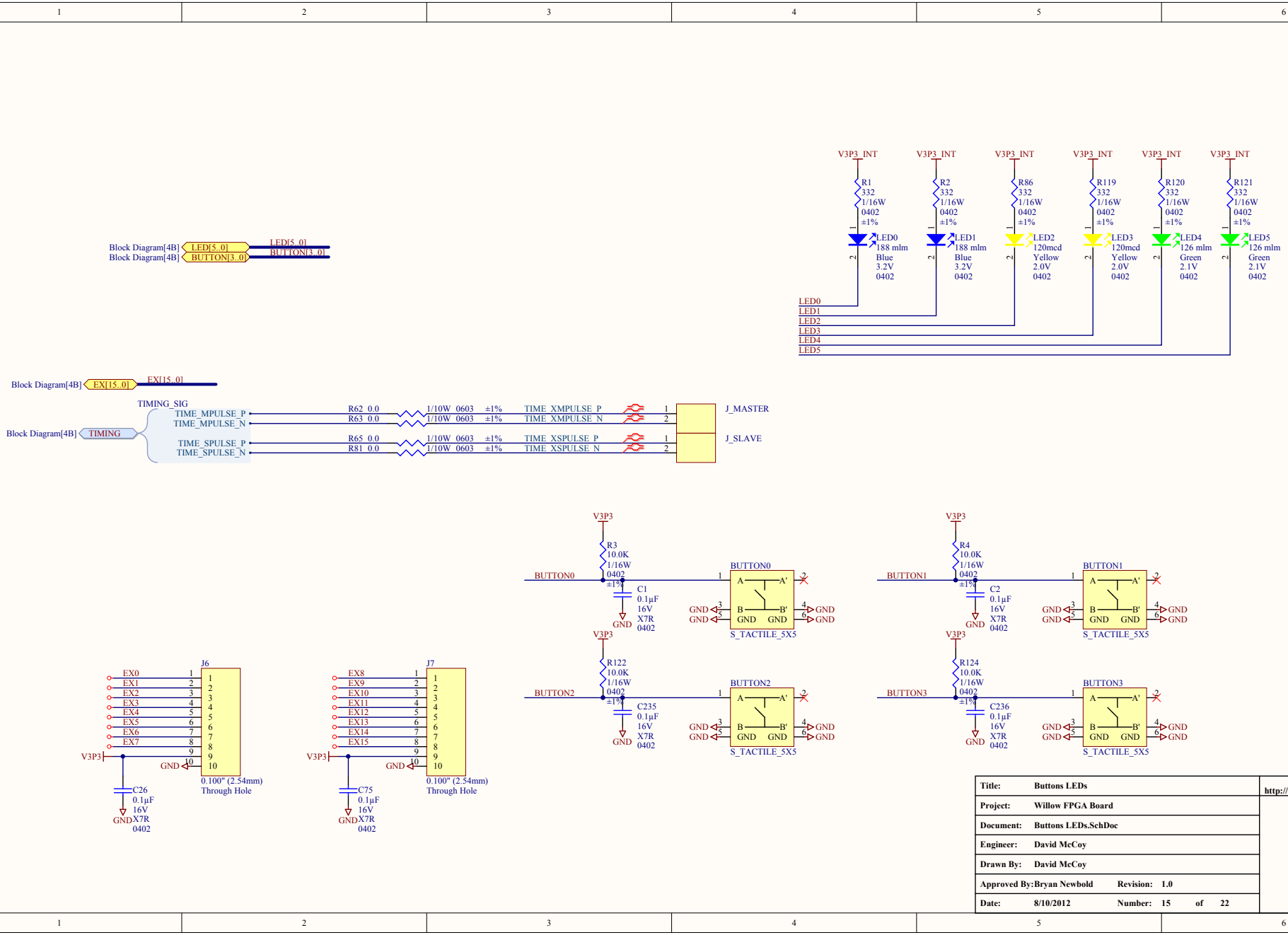


Title:	**Wired Leaf DAQ Interface**		**Leaf Labs http://www.leaflabs.com**
Project:	**Willow FPGA Board**		
Document:	**DAQ Interface.SchDoc**		
Engineer:	**David McCoy**		
Drawn By:	**David McCoy**		
Approved By:	**Bryan Newbold**	**Revision:** **1.0**	
Date:	**8/10/2012**	**Number:** **12** **of** **22**	

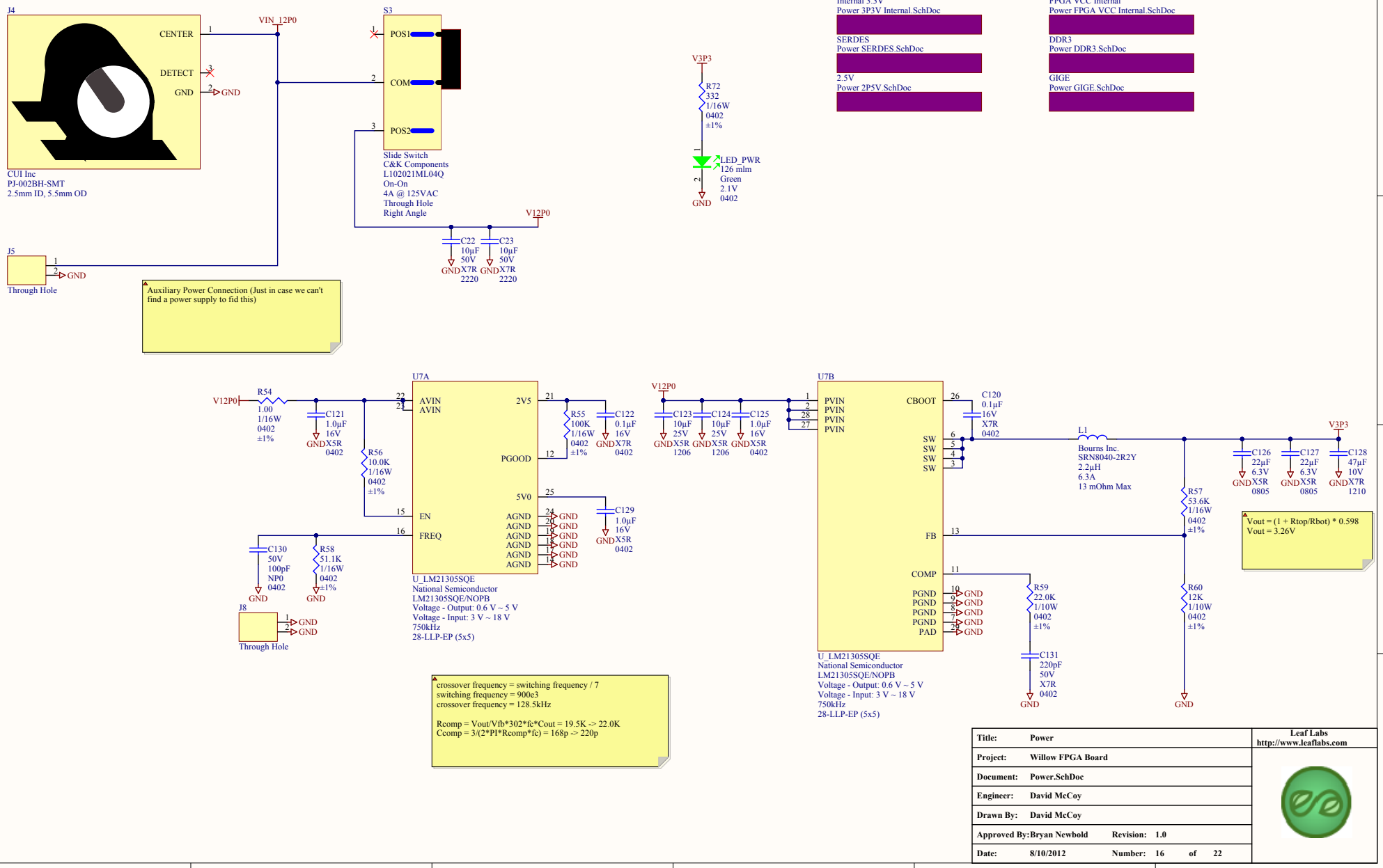

Detect Pins
T1
T2
U20A
Marvell PHY
Marvell
88E1111-XX-RCJXX
128P PQFP
In SGMII Mode S_CLK becomes serial detect inputs
TXD4 - TXD7 Cannot be left floating! these must tied high or low
U20B
Marvell PHY
Marvell
88E1111-XX-RCJXX
128P PQFP
J12
10/100/1000 RJ45 W/ MAG and LEDs
TE Connectivity
6605444-6
SGMII_DATA_Harness
MAC_CONTROL_Harness
Harness
MDC and MCIO are 3.3V Tolerant
SEL_FREQ: Selects the input frequence of the clock on XTAL1
NC/High: 25MHz
**** Low: 125MHz
U20C
Marvell PHY
Marvell
88E1111-XX-RCJXX
128P PQFP
U20D
Marvell PHY
Marvell
88E1111-XX-RCJXX
128P PQFP
There is a discrepency between the reference design and the datasheet
For SGMII to use the inferred clock from the data lines use jumper select 2 - 3, but the reference design it would use 1 - 2 so I'm leaving both of them in the design just in case
U18
125MHz Oscillator
125MHz
CMOS
1.8 V ~ 3.3 V
±10ppm
16mA
4-SMD, No Lead (DFN, LCC)
3.3V - 2.5V level translator
I\N\T\ Pin is open drain so it will interface with 3.3V Bank
Interrupt pin is active low
Configuration Settings
Pin to Constant Map
Title: Gigabit Ethernet
Project: Willow FPGA Board
Document: GIGE.SchDoc
Engineer: David McCoy
Drawn By: David McCoy
Approved By: Bryan Newbold
Revision: 1.0
Date: 8/10/2012
Number: 13 of 22
Leaf Labs
http://www.leaflabs.com



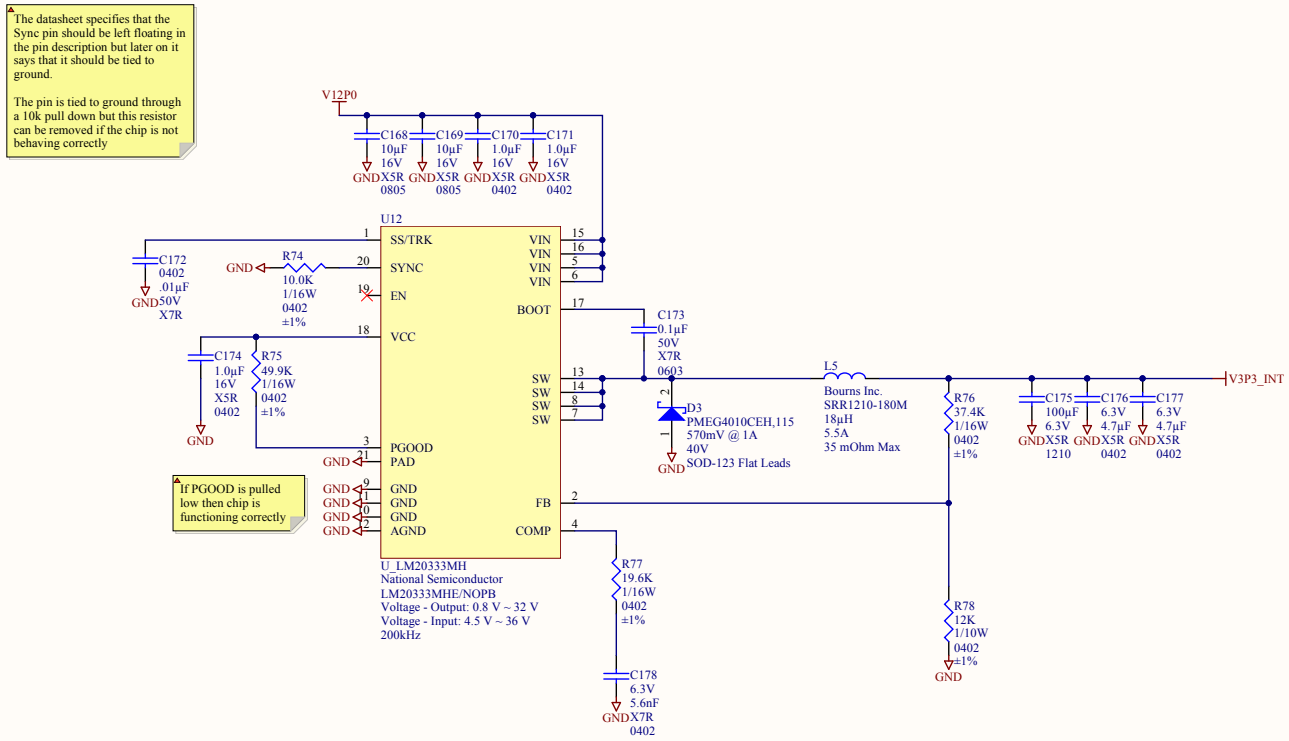
Title:	**Maple Mini**		**Leaf Labs http://www.leaflabs.com**
Project:	**Willow FPGA Board**		
Document:	**Maple Mini.SchDoc**		
Engineer:	**David McCoy**		
Drawn By:	**David McCoy**		
Approved By:	**Bryan Newbold**	**Revision:**	**1.0**
Date:	**8/10/2012**	**Number:**	**14 of 22**



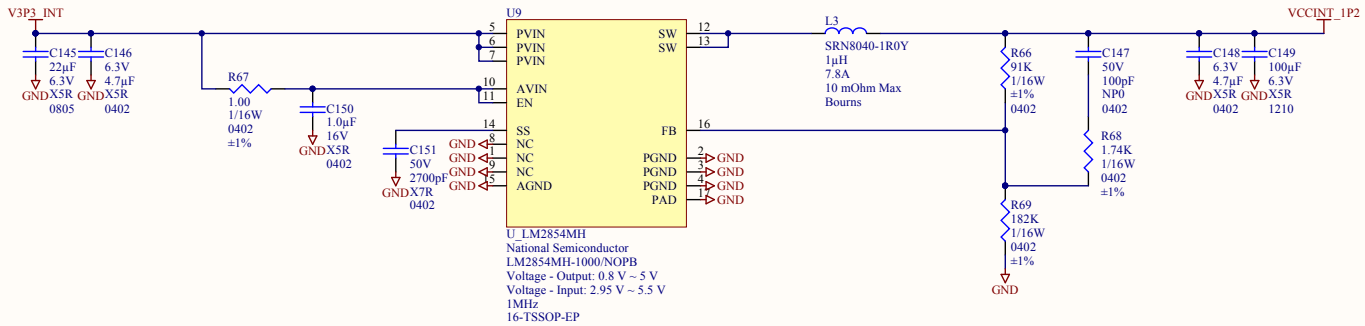
Title:	**Buttons LEDs**		**Leaf Labs http://www.leaflabs.com**
Project:	**Willow FPGA Board**		
Document:	**Buttons LEDs.SchDoc**		
Engineer:	**David McCoy**		
Drawn By:	**David McCoy**		
Approved By:	**Bryan Newbold**	**Revision:** **1.0**	
Date:	**8/10/2012**	**Number:** **15** **of** **22**	



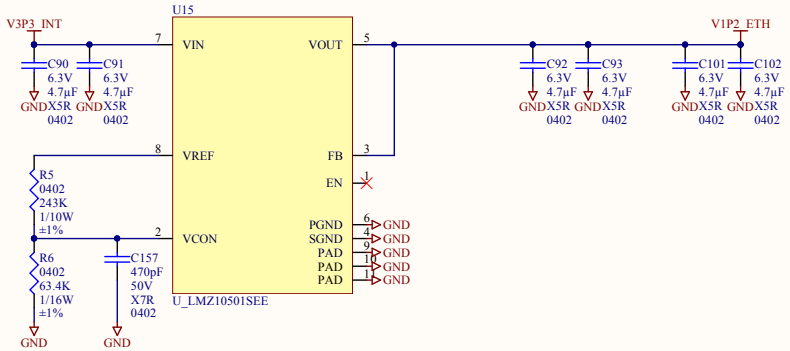
Title:	**Power**		**Leaf Labs http://www.leaflabs.com**
Project:	**Willow FPGA Board**		
Document:	**Power.SchDoc**		
Engineer:	**David McCoy**		
Drawn By:	**David McCoy**		
Approved By:	**Bryan Newbold**	**Revision:** **1.0**	
Date:	**8/10/2012**	**Number:** **16** **of** **22**	



Title:	Power Internal 3.3V			Leaf Labs http://www.leaflabs.com
Project:	Willow FPGA Board			
Document:	Power 3P3V Internal.SchDoc			
Engineer:	David McCoy			
Drawn By:	David McCoy			
Approved By:	Bryan Newbold	Revision:	1.0	
Date:	8/10/2012	Number:	17 of 22	



Title:	**Power FPGA VCCINT**				**Leaf Labs http://www.leaflabs.com**
Project:	**Willow FPGA Board**				
Document:	**Power FPGA VCC Internal.SchDoc**				
Engineer:	**David McCoy**				
Drawn By:	**David McCoy**				
Approved By:	**Bryan Newbold**	**Revision:**	**1.0**		
Date:	**8/10/2012**	**Number:**	**18**	**of**	**22**



Title:	Power FPGA SERDES				Leaf Labs http://www.leaflabs.com
Project:	Willow FPGA Board				
Document:	Power GIGE.SchDoc				
Engineer:	David McCoy				
Drawn By:	David McCoy				
Approved By:	Bryan Newbold	Revision:	1.0		
Date:	8/10/2012	Number:	19	of 22	

Enable all regulators for the DDR2

Enable the S3 for the DDR2 for the FPGA.

Put the sense voltage for the VTT close to the DDR3 FPGA

Pin Functions, and uses

COMP: Outptu of the transconductance amplifier, since I'm not using a current feedback loop this is attached to V5IN which puts the device in D-CAP mode (no current sense)

MODE: Discharge Mode setting pin (Connected to VLDOIN. This discharges the VTT through the internal LDO. This is a moot point because there is no way to turn off the device because the S3, and S5 pins are permanently enabled

V12P0
C86 4.7µF 25V X5R 0805
GND
U13
VIN VOUT_1.2V
GND TAB=VOUT_1.2V
5V
TO-252-3
Diodes Inc
ZLDO1117K50TC
Positive Fixed
Up to 18V
1.11V @ 1A
V5P0
C89 4.7µF 25V X5R 0805

U8C
V5P0_FILT R79 4.32K ±1% 1/10W 0402
V5P0
CS COMP PGOOD
V3P3_INT R83 10.0K 1/16W 0402 ±1%
S5 S3 NC NC
DDR2 Buck Regulator
Texas Instruments
TPS51116RGER
3 V ~ 28 V
1.5 V ~ 3 V
24-VFQFN Exposed Pads

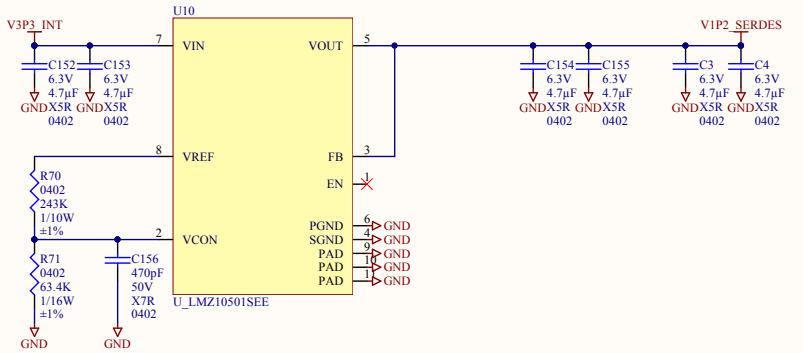
V12P0
C132 10µF 25V X5R 1206
C133 10µF 25V X5R 1206
C134 1.0µF 50V X7R 0805
GND

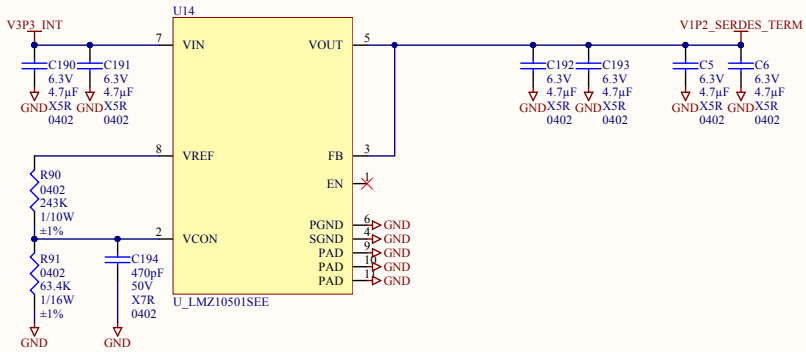
U8A
DRVH VBST LL DRVL PGND CS_GND VDDQSNS VDDQSET GND PAD
C135 0.1µF 16V X7R 0402
Q1
Q2
8.2 mOhm @ 17A, 10V
25V
60A
2.3V @ 250µA
5.6nC @ 4.5V
8-SON
L2
HC7-1R0-R
1µH
8A
6.5 mOhm Max
Wurth
C136 22µF 6.3V X5R 0805
C137 100µF 6.3V X5R 1210
C138 100µF 6.3V X5R 1210
C139 100µF 6.3V X5R 1210
V1P5
R94 ±1% 22 1/4W 1206
GND
R92 75K 1/10W 0402 ±1%
R93 75K 1/10W 0402 ±1%
VTT_LDO_IN
DDR2 Buck Regulator
Texas Instruments
TPS51116RGER
3 V ~ 28 V
1.5 V ~ 3 V
24-VFQFN Exposed Pads

V5P0
C141 6.3V 4.7µF X5R 0402
R64 5.1 1/16W 0402 ±1%
V5P0_FILT
C142 1.0µF 16V X5R 0402
VTT_LDO_IN

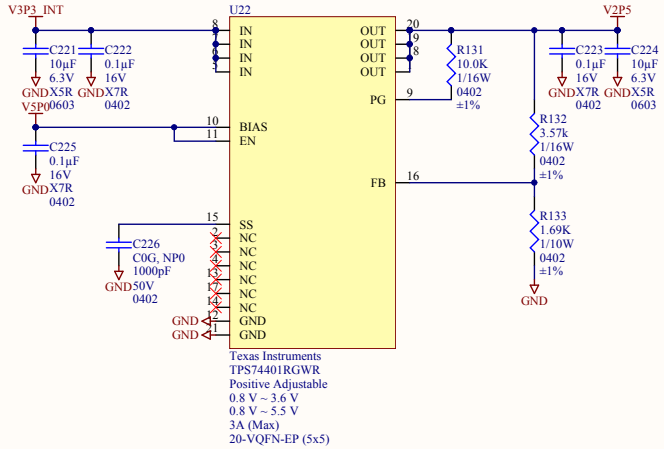
U8B
V5IN V5FILT VLDOIN MODE VTTREF VTT VTTSNS VTTGND
DDR_VREF
C140 0.033µF 16V X7R 0402
DDR_VTT
C143 10µF 25V X5R 1206
C144 10µF 25V X5R 1206
GND
DDR2 Buck Regulator
Texas Instruments
TPS51116RGER
3 V ~ 28 V
1.5 V ~ 3 V
24-VFQFN Exposed Pads

Title:	Power DDR3		Leaf Labs http://www.leaflabs.com
Project:	Willow FPGA Board		
Document:	Power DDR3.SchDoc		
Engineer:	David McCoy		
Drawn By:	David McCoy		
Approved By:	Bryan Newbold	Revision: 1.0	
Date:	8/10/2012	Number: 20 of 22	

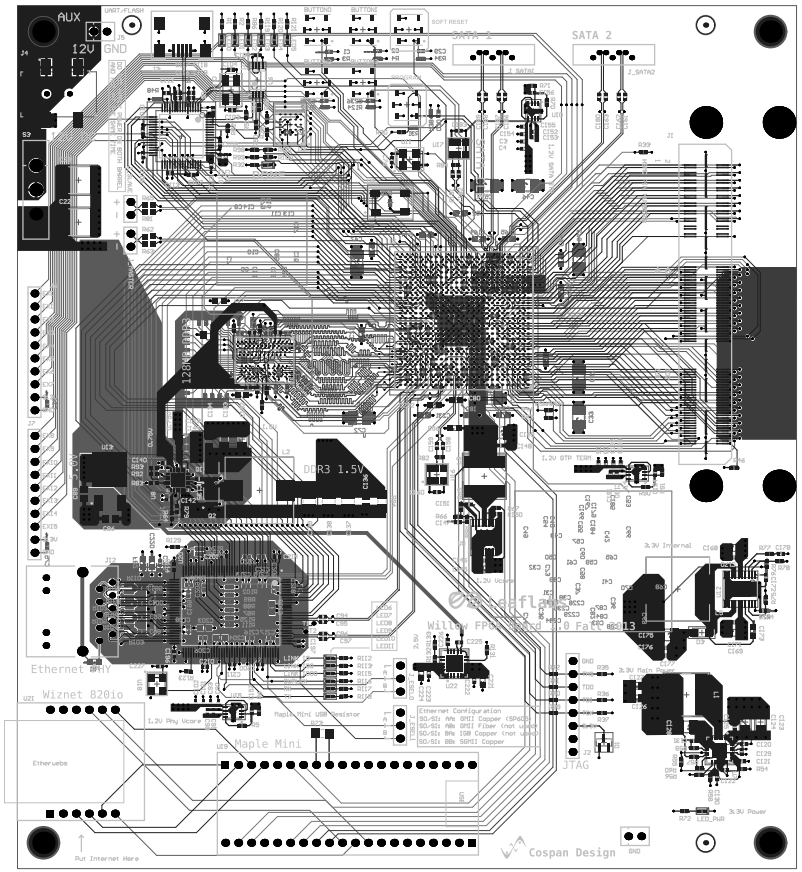




Title:	Power FPGA SERDES				Leaf Labs http://www.leaflabs.com
Project:	Willow FPGA Board				
Document:	Power SERDES.SchDoc				
Engineer:	David McCoy				
Drawn By:	David McCoy				
Approved By:	Bryan Newbold	Revision:	1.0		
Date:	8/10/2012	Number:	21	of 22	



Title:	**Power 2.5V**			**Leaf Labs http://www.leaflabs.com**
Project:	**Willow FPGA Board**			
Document:	**Power 2P5V.SchDoc**			
Engineer:	**David McCoy**			
Drawn By:	**David McCoy**			
Approved By:	**Bryan Newbold**	**Revision:**	**1.0**	
Date:	**8/10/2012**	**Number:**	**22 of 22**	



Layer Stack Up Detail for: SNG_PCB.PcbDoc			
Layer			
Name			
S_TOP			
GND1			
S1			
P1			
P2			
S2			
GND2			
S_BOT			

Fabrication Notes
1. Overall board height: 62mils
2. 20mil pullback on inner planes
3. Tent all vias under BGA (Top Side only)
4. 1.5 Oz copper on top and bottom
5. 1.0 Oz copper on internal signal, power and ground layers
6. Controlled Impedance: Internal layers Single Ended 4.7mil trace = 50 Ohms
7. Controlled Impedance: External Layers Single Ended 4.7mils = 50 Ohms
8. Controlled Impedance: Internal Layers Differential 4mil trace 10 mil sep = 100 Ohms
9. Controlled Impedance: External Layers Differential 4mil trace 12 mil sep 100 Ohms

Design Notes
1. Unless otherwise stated all dimensions are in mils

LAYER - GERBER LAYERS - DESCRIPTION

GTL – TOP LAYER
GTO – TOP SILKSCREEN

G1 – INNER LAYER 1

G2 – INNER LAYER 3

GBL – BOTTOM LAYER
GBO – BOTTOM SILKSCREEN

MECHANICAL LAYERS
01 Component Outline
02 PCB BOUNDRY

06 FABRICATION NOTES
07 Component Designators
08

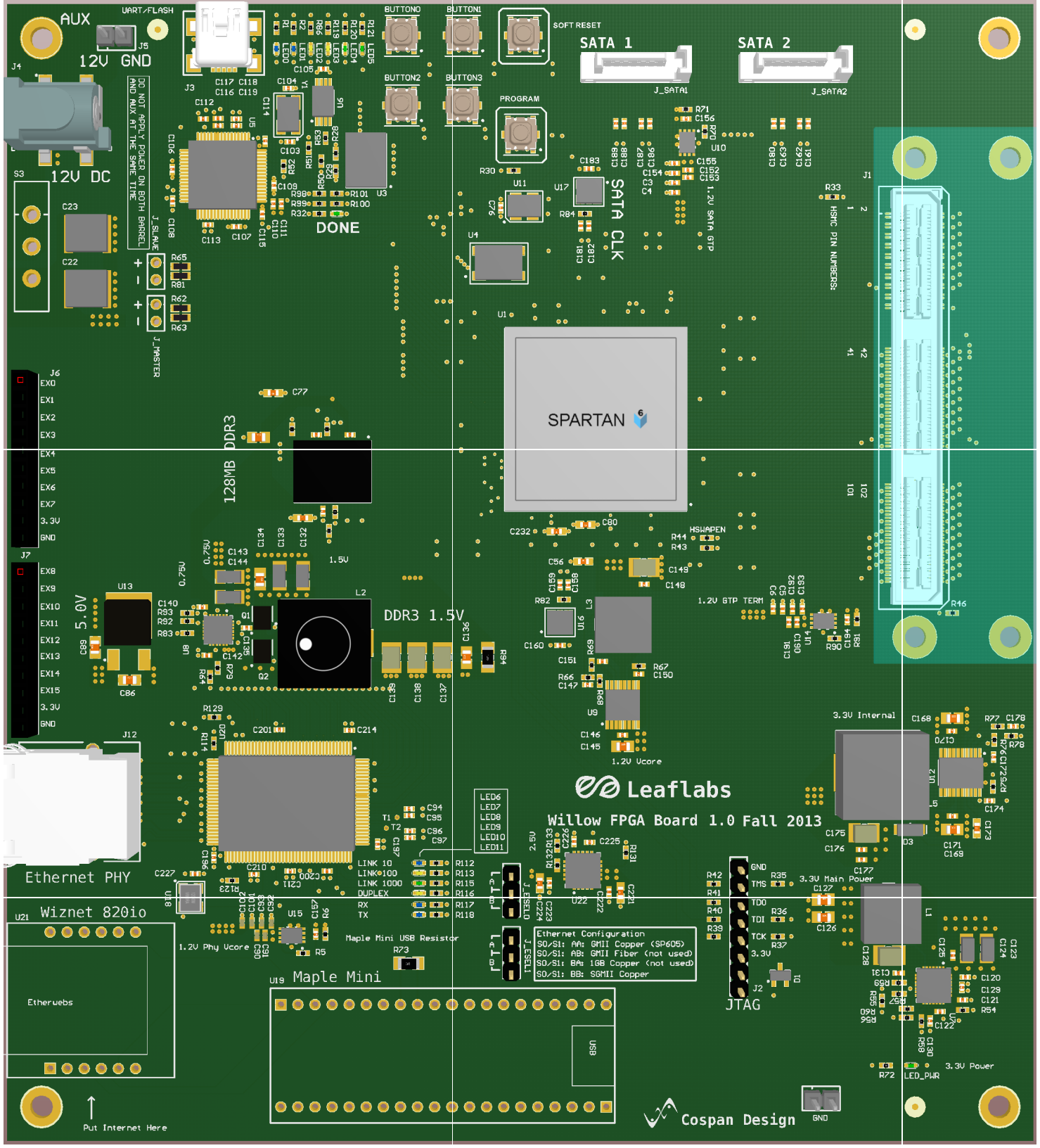
11 DESIGN INFORMATION

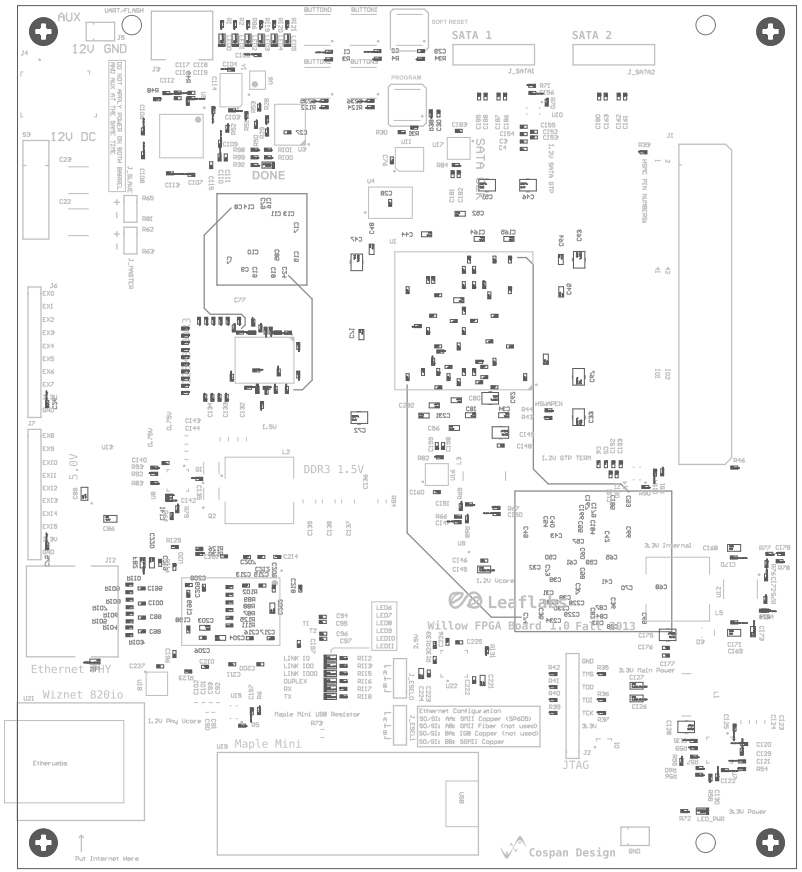
13 Height Information

15 ASSEMBLY
16 SHEET

MULTI-LAYER HOLES

Dave McCoy	Leaflabs LLC		
Dave McCoy			
3/16/2015	Wired Leaf	3/16/2015	1.0
B Size 1:1	Willow FPGA Board.PcbDoc	Sheet 1	of 1


AUX
12V GND
UART/FLASH
J5
J4
12V DC
DO NOT APPLY POWER ON BOTH BARREL AND AUX AT THE SAME TIME
J_SLAVE
J_MASTER
S3
BUTTON0
BUTTON1
BUTTON2
BUTTON3
SOFT RESET
PROGRAM
SATA 1
SATA 2
J_SATA1
J_SATA2
SATA CLK
1.2V SATA GTP
HSMC PIN NUMBERS:
DONE
SPARTAN 6
DDR3
128MB
DDR3 1.5V
1.5V
0.75V
5.0V
HSWAPEN
1.2V GTP TERM
1.2V Vcore
3.3V Internal
3.3V Main Power
3.3V Power
Leaflabs
Willow FPGA Board 1.0 Fall 2013
Ethernet PHY
Wiznet 820io
Etherwebs
1.2V Phy Vcore
Maple Mini USB Resistor
Maple Mini
USB
LINK 10
LINK100
LINK 1000
DUPLEX
RX
TX
Ethernet Configuration
SO/S1: AA: GMII Copper (SP605)
SO/S1: AB: GMII Fiber (not used)
SO/S1: BA: 1GB Copper (not used)
SO/S1: BB: SGMII Copper
JTAG
GND
TMS
TDO
TDI
TCK
3.3V
LED_PWR
Put Internet Here
Cospan Design



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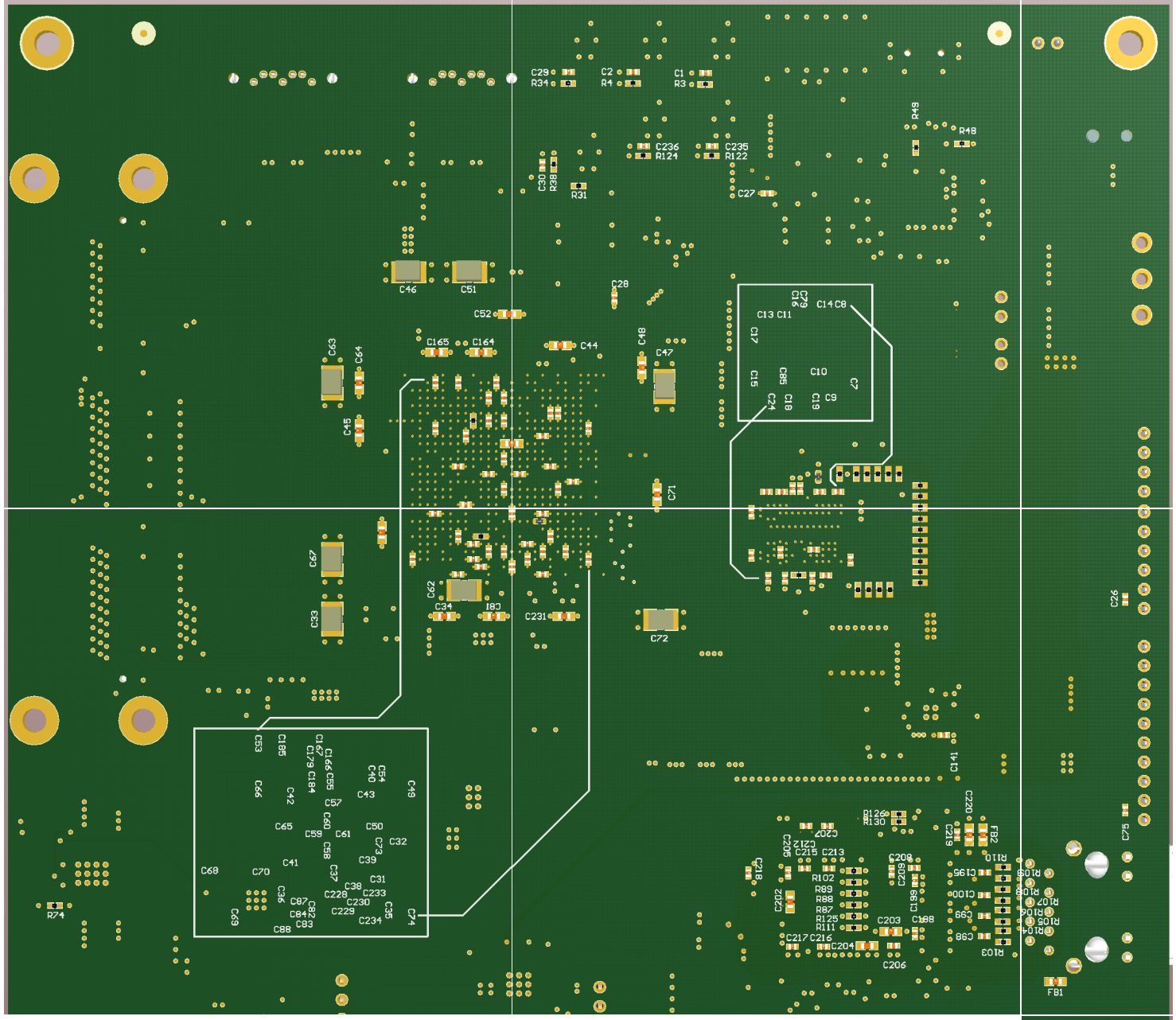

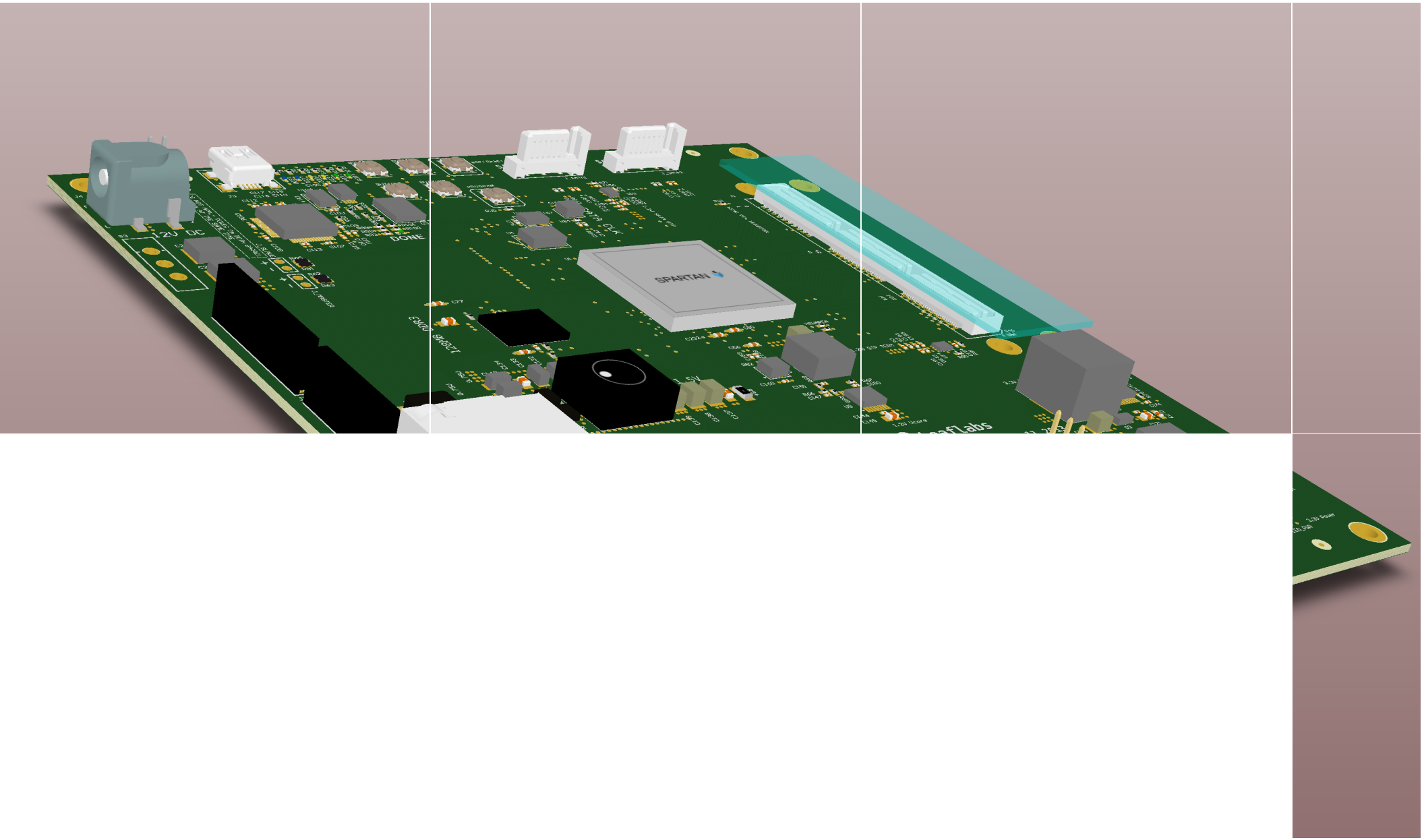
12V DC
SPARTAN